

Novel electronic devices using smart piezoelectric/electrostrictive materials

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Power dissipation is one of the most challenging factors for continued semiconductor transistor scaling in the evolution of integrated circuits. The heat generation due to large power dissipation density restricts the device scaling in integrated circuits (ICs). To circumvent this power crisis in ICs, it requires exploring new materials/device structures and operating principles. The goal is to design transistor switch in a way that the device dissipates less power during logic operation than conventional FETs, BJTs. To meet this requirement, it has been suggested to reduce the conventional subthreshold slope (SS) limit below 60 mV/decade at room temperature. Here, we propose a novel transistor switch that exploits electrostriction and piezoelectricity in piezoelectric/electrostrictive active gate barriers of transistors. Using the smart materials as the barriers of parallel-plate capacitor, we first analytically showed how one can obtain positive and negative differential capacitance in piezoelectric capacitor based on the physics of Gauss' electrostatics and electrostriction. Furthermore, by using this piezoelectric capacitor in the gate capacitor of a transistor, we also showed, by exploiting negative barrier capacitance, how one can achieve an ON-current boost, a higher transconductance/gain, and a steep subthreshold switching ($SS < 60$ mV/decade) in transistors. Finally experimental results for C-Vs, I-Vs of capacitors and transistors with steep $SS \sim 46$ mV/decade, and $I_{ON}/I_{OFF} \sim 10^9$ using MBE-grown III-nitride piezoelectric heterostructures such as $In_{0.17}Al_{0.83}N/AlN/GaN$ HEMTs with piezoelectric barrier layer thickness of ~ 2.5 nm and 5 nm will be presented and discussed. In conclusion, this proposed novel devices have potential applications in energy-efficient, high-performance, digital and RF nanoelectronics.

Biography:

Dr. Raj K Jana is an Advisory Engineer of advanced nanoscale CMOS device division at IBM Semiconductor Research & Development Center, NY, USA, and Research Associate in Electrical Engineering Department at University of Notre Dame, IN, USA. He received his B.E. degree in Electronics and Telecommunication Engineering from Bengal Engineering and Science University, India, and Ph.D. in Electrical Engineering, at University of Notre Dame, 2015. Prior to Ph.D. program, from 2008 to 2009, he was with STMicroelectronics, India, where he worked on System-on-Chip design, validation based on 45-nm CMOS technology node. From 2006 to 2008, he was with the Samtel R&D Center, India, where he worked as a design engineer on the development of efficient electronic driving systems in plasma display technology. His research interests include the device physics, carrier transport, the development of novel high-performance energy-efficient electronic devices (capacitors, transistors) using III-V nitride semiconductors, and 2D materials for energy-efficient applications.